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Crafts

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(54) **SEA-OF-CELLS ARRAY OF TRANSISTORS**

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(58) **Field of Search** 257/211, 207, 257/369, 377, 758

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,461,361 A	*	8/1969	Delivorias	257/369
4,143,178 A		3/1979	Harada et al.	427/85
4,151,635 A		5/1979	Kashkooli et al.	29/571
4,229,756 A		10/1980	Sata et al.	357/42
4,244,001 A		1/1981	Ipri	357/44
4,317,690 A		3/1982	Koomen et al.	148/187
4,525,809 A		7/1985	Chiba et al.	365/51
4,584,653 A		4/1986	Chih et al.	364/491
4,593,205 A		6/1986	Bass et al.	307/269
4,630,219 A		12/1986	DiGiacomo et al.	364/488
4,638,458 A		1/1987	Itoh	365/51
4,682,202 A		7/1987	Tanizawa	357/45
4,686,758 A		8/1987	Liu et al.	437/34
4,701,642 A		10/1987	Pricer	307/446
4,845,544 A		7/1989	Shimizu	357/71
4,849,344 A		7/1989	Desbiens et al.	437/31
4,905,073 A		2/1990	Chen et al.	357/67
4,989,062 A		1/1991	Takahashi et al.	357/45
4,999,518 A		3/1991	Dhong et al.	307/446
5,003,199 A		3/1991	Chuang et al.	307/446
5,008,208 A		4/1991	Liu et al.	437/31
5,013,679 A		5/1991	Kumagai et al.	437/52
5,032,530 A		7/1991	Lowrey et al.	437/34
5,037,766 A		8/1991	Wang	437/24
5,045,726 A		9/1991	Leung	307/466
5,049,515 A		9/1991	Tzeng	437/43
5,081,518 A		1/1992	El-Dwany et al.	357/59
5,124,776 A		6/1992	Tanizawa et al.	357/45
5,126,279 A		6/1992	Roberts	437/52
5,162,884 A		11/1992	Liou et al.	257/384
5,168,072 A		12/1992	Moslehi	437/41
5,175,118 A		12/1992	Yoneda	437/40

(List continued on next page.)

OTHER PUBLICATIONS

IBM Technical Dislosure Bulletin; vol. 25, No. 4; Sep. 1982; Structured Macro; E.H. Stoops.

An Efficient Algorithm for some Mltirow Layout Problems; J. Feldman et al.; IEEE Transactoinson Computer–Aided Design of Integrated Circuits & Systems; vol. 12, No. 8, Aug. 1993; pp. 1178–1185.

10K–Gate GaAs JFET Sea of Gates; H. Kawasaki et al.; IEEE Journal of Solid–State Circuits; vol. 26, No. 10; Oct. 1991; pp. 1367–1370.

A Comprehensive CAD System for High–Performance 300K–Circuit ASIC Logic Chips; J. Panner et al.; IEEE Journal of Solid–State Circuits; vol. 26, No. 3; Mar. 1991; pp. 300–309.

(List continued on next page.)

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(57) **ABSTRACT**

The invention concerns integrated circuits in which a MACRO is embedded in a standard cell array. One level of metal is devoted exclusively to non-local interconnect, and a layer of polysilicon is devoted to local interconnect, thereby saving significant space.

10 Claims, 12 Drawing Sheets